

ABSTRACT

A single-path delay feedback pipelined fast Fourier transform processor comprising at least one set of triplet FFT stage means: a first FFT stage means comprising a radix-2 butterfly, a feedback memory, and a multiplication by unity; a second FFT stage means comprising a trivial coefficient pre-multiplication, a radix-2 butterfly, a feedback memory, and a multiplication by selectable unity or $W_N^{N/8}$; and a third FFT stage means comprising a trivial coefficient pre-multiplication, a butterfly, a feedback memory, and a complex twiddle coefficient multiplication with coefficients determined using a twiddle factor decomposition technique.